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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE	
In re Application of: Cecchi, et al. Serial No. 09/903,239 Filed: 07/11/01 For: "CMOS Low Voltage High-Speed Differential Amplifier"	Group Art Unit: 2816 Examiner: NGUYEN, LONG T
SUBMISSION UNDER 37 CFR §1.114(c)	

9/30/03
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AFFIDAVIT UNDER 37 C.F.R. §1.132

1. My name is Curtis Walter Preuss. I am over twenty-one years old and I make the following declaration based on my own personal knowledge.
2. I am an engineer with IBM and a co-inventor of the present invention in the above identified U.S. Patent Application.
3. I have performed a comparative computer simulation between a first electrical circuit of the present invention illustrated in FIG. 2 of the above identified patent application, and a second electrical circuit illustrated in FIG. 2 of U.S. Patent Serial No. US 6,313,696B1 to Zhang, Differential buffer Having Common-Mode Rejection, issued on 11/6/2001. Attached are three attachments illustrating testing circuits and test results.
4. Attachment A illustrates the layout for the comparative computer simulation, where the first electrical circuit (corresponding to the present invention) is in the upper portion and has an output labeled as OUT and the second electrical circuit (corresponding to the circuit disclosed in Zhang) is in the lower portion and has an output labeled as OUT1.
5. Attachment B illustrates the measurements for OUT (present invention) and OUT 1 (Zhang). It can be observed that OUT1 (Zhang) has more distortion and OUT (present invention) has more symmetrical rise and fall time. In a high speed data link application, the distortion presented by OUT1 (Zhang) would add jitter and make the signal less reliable. It should also be noted that OUT1 (Zhang) has less bandwidth throughout and that OUT1's (Zhang's) amplitude shrinks noticeably as the speed increases.

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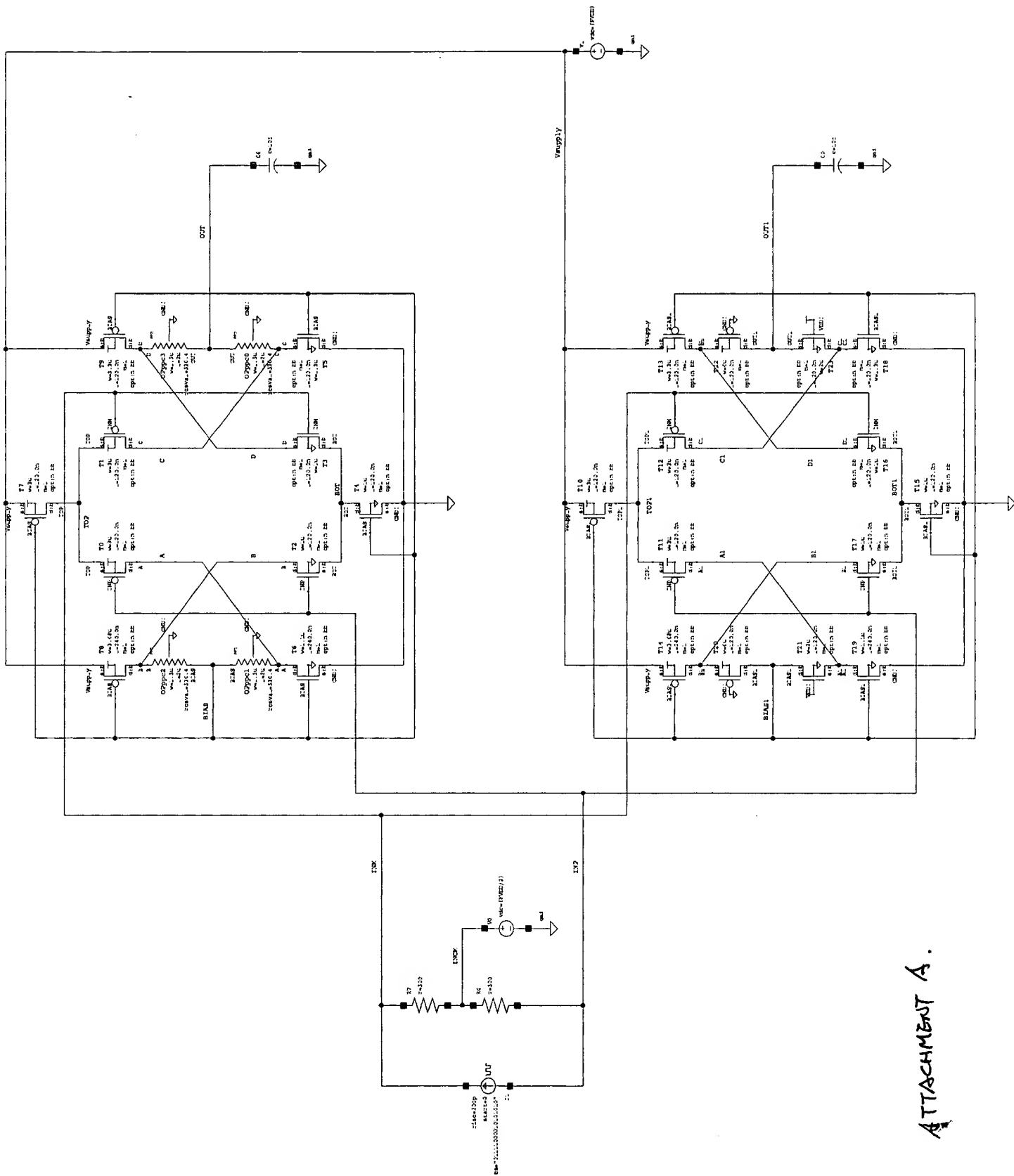
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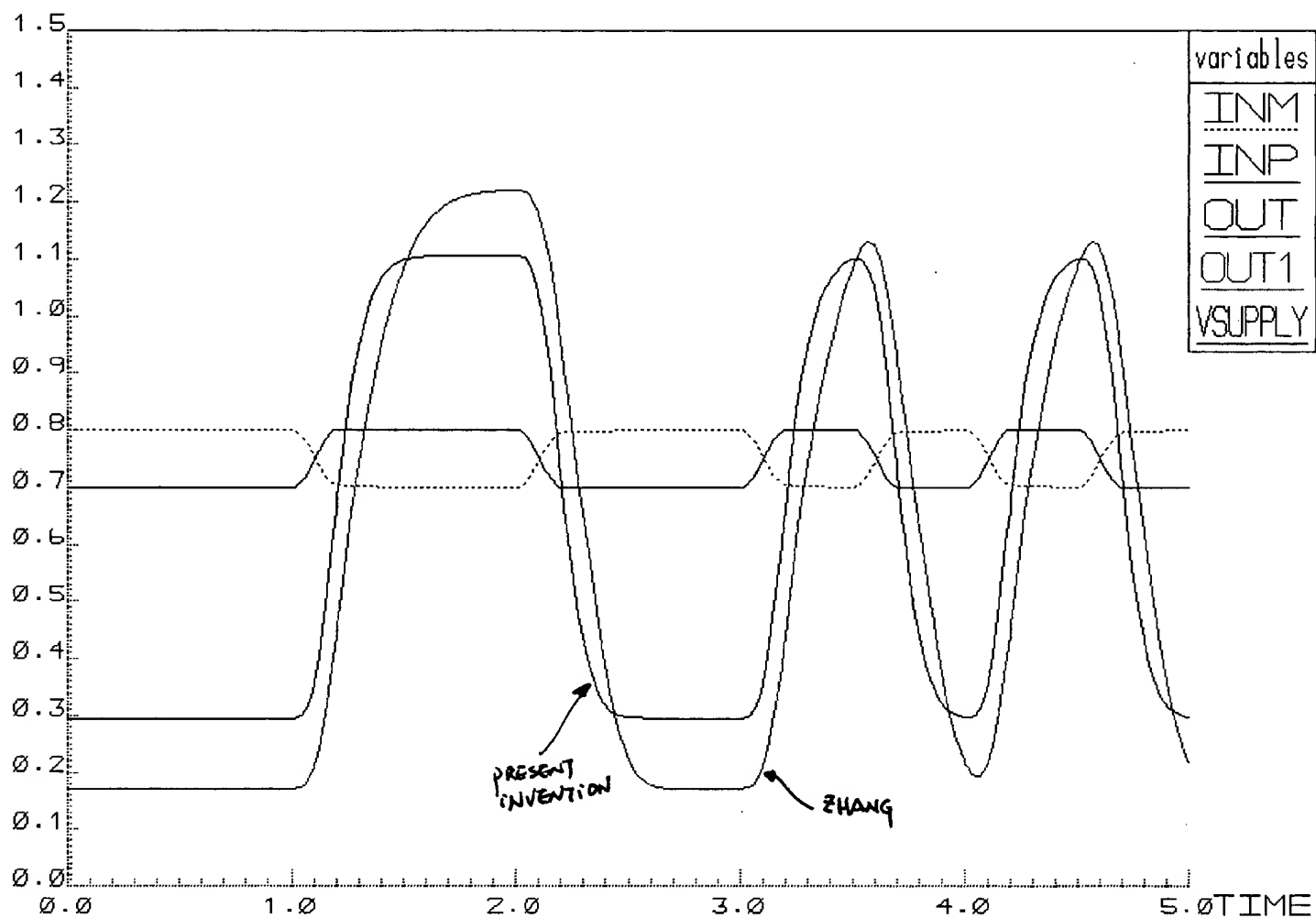
6. Attachment C illustrates 3 figures: FIG. 1, FIG. 2, and FIG. 3. FIGs. 1, 2, and 3 illustrate measurements taken simultaneously at different points in two circuits shown in Attachment A, where FIG. 3 is a repeat of Attachment B's illustration.
7. FIG. 1 illustrates drain and source voltage at FET T23 (Zhang) in the second electrical circuit in the lower portion of Attachment A. The y-axis represents the voltage.
8. FIG. 2 illustrates a resistance comparison between a FET (PRF) (Zhang) and a resistance (PRR) (present invention) of the first electrical circuit in the upper portion of Attachment A. The y-axis represents the variance in resistance.
9. It is observed in FIG. 3 that the resistance PRF (Zhang) at a FET's channel changes substantially when the channel is submitted to a large voltage range (see the corresponding voltage variance in FIG. 1), while the resistance PRR (present invention) remains at a constant level.
10. The circuit of the invention has the advantage of providing constant resistance over a variety of voltages, whereas the circuit disclosed in Zhang does not. Therefore, the electrical circuit of the present invention and the electrical circuit of Zhang are not equivalent.



Curtis Walter Preuss



ATTACHMENT A.



ATTACHMENT B.

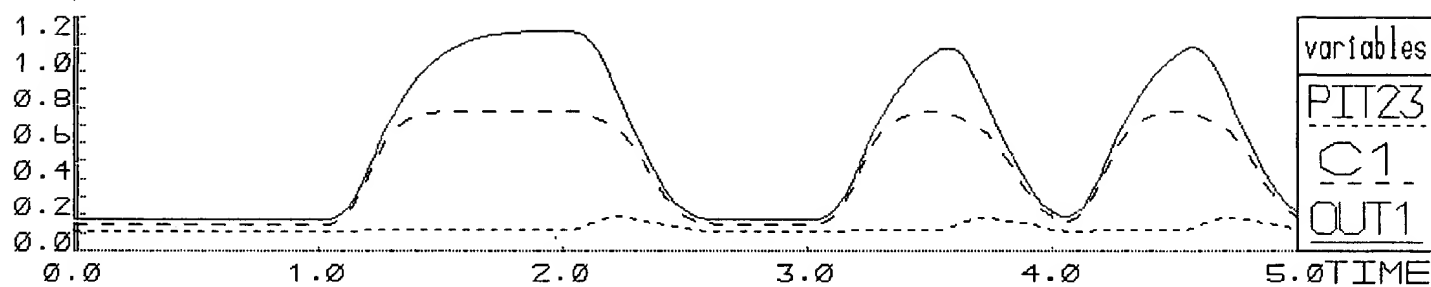


FIG. 1

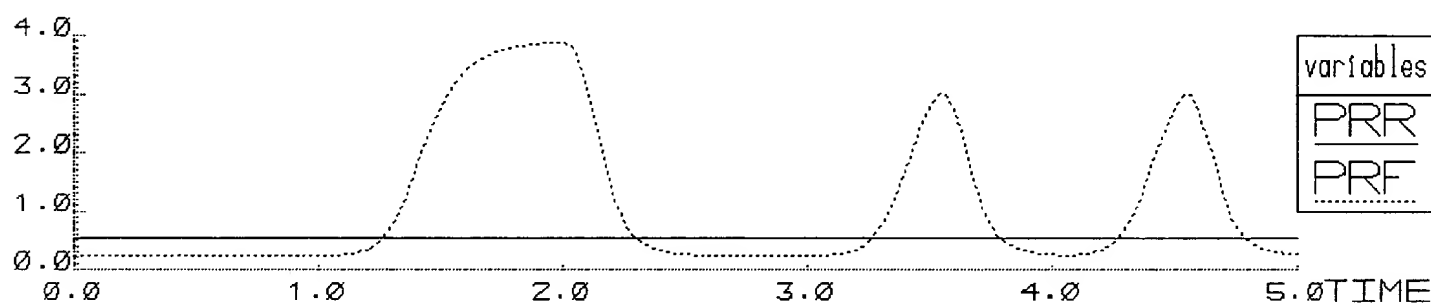


FIG. 2

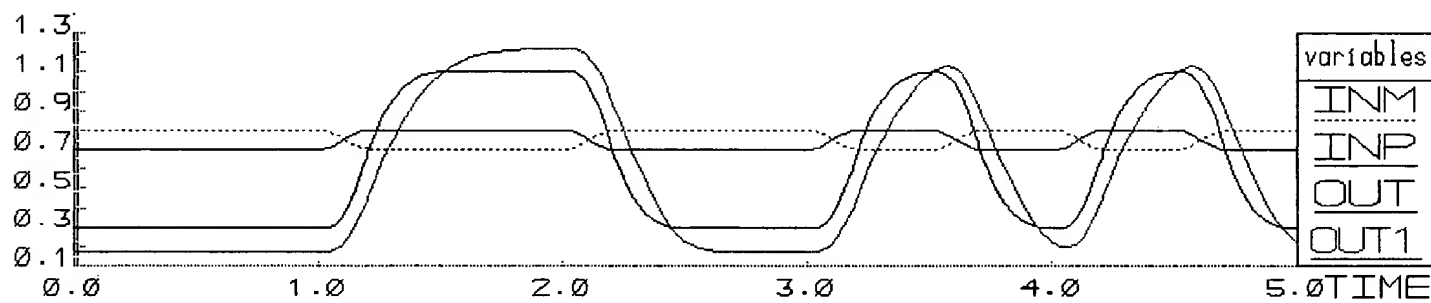


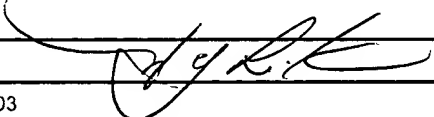
FIG. 3


ATTACHMENT C.

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/903,239	
	Filing Date	7/11/01	
	First Named Inventor	Cecchi, et al.	
	Art Unit	2816	
	Examiner Name	Long T. Nguyen	
Total Number of Pages in This Submission	14	Attorney Docket Number	18244.2

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